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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,918	06/09/2000	Stefanos Kaxiras	2-2	3479

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EXAMINER	
GOSSAGE, GLENN A	

ART UNIT	PAPER NUMBER
2187	7

DATE MAILED: 09/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/591,918	KAXIRAS ET AL.	
	Examiner	Art Unit	
	Glenn Gossage	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-34 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-34 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 09 June 2000 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5,6 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. The abstract of the disclosure is objected to because it does not enable one to quickly determine from a cursory inspection the nature and gist of the technical disclosure as required by 37 CFR 1.72(b). Initially, it appears an introductory sentence such as --A multiprocessor system, apparatus and method for determining a set of predicted readers of a data block in a shared-memory multiprocessor system, are disclosed.-- should be inserted before "A set" in line 1 (page line 2) for clarity and completeness (note claims 1 and 22, lines 1-2 and claim 28, line 1, e.g.). Also, it appears "A" in line 1 (page line 2) should then be changed to --The--.

Additionally, while the Examiner appreciates the comprehensive nature of the abstract, the abstract is somewhat long, particularly in light of the newer 150 word/15 line limit. The following changes are suggested to shorten the abstract while not substantively changing its content.

In line 1 (page line 2), delete "are determined." In lines 1-3 (page lines 2-4), change "in a shared ... predicted readers based on the" to simply --is generated based on a--. In (page) line 6, change "In ..., the" to simply --The--, and change "are" to --may be--. In (page) line 7, after "function" insert -- , such as a union, intersection or pattern-based function, --, and in (page) lines 8-10, delete "The function ... system." In (page) lines 10-11, change "of the directory comprises" to --may comprise--, and in line 11, delete "processed by the directory." In line 12, delete "of previous readers" and in lines 12-13, delete "associated ... predicted readers." In lines 13-14, change "use additional ... such as" to --also use--. In line 15, after "identification," insert --(ID)--.

Appropriate correction is required. See MPEP § 608.01(b).

2. The drawings are objected to because in Figures 1 and 2, it appears "NI" within "boxes" 104A-C should be changed to --Net. I/F-- or --Network I/F-- for clarity (since the acronym or abbreviation "NI" does not appear to be "well known" or commonly used in the art).

In Figure 4, the wording "processors in the set {a, b, c}" is somewhat confusing. It appears "processors in the set {a, b, c}" should be changed to --processors in the set of nodes {a, b, c}-- for clarity and consistency (see page 7, lines 5-6, e.g.).

In Figure 5, within step or "box" 202, it appears --current-- should be inserted before "readers" for clarity and consistency (see page 7, line 15). In step or "box" 212, it appears "registers" should be --register-- (see page 7, line 23). In step or "box" 216, the wording "predicts a function" is unclear and confusing (in this regard, also see the objection below with respect to page 7, line 24). It appears "predicts a function of the sets" should be changed to --predicts a set of readers-- (see page 9, lines 8-12 as well as the wording in step or "box" 224), and "(intersect or union)" changed to --(intersection or union function)-- (see page 8, line 7, e.g.), for clarity and consistency.

Applicant is REQUIRED to submit a proposed drawing correction in response to this Office action. However, actual formal correction of the noted defect(s) (submission of corrected formal drawings, e.g.) can be deferred until the application is allowed by the examiner.

Also note MPEP 608.02(r) and (v).

4. The disclosure has not been checked by the Examiner to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the disclosure. The following objections are specifically noted:

In the specification:

On page 1, line 12, it appears "state" should be --states-- or --a state-- for clarity.

On page 2, line 27, "are" should be --is-- ("set ... is." Note lines 24-25.).

On page 4, line 26, it appears "one" should be --two-- for clarity. [Note that while an applicant may generally be his or her own lexicographer, no term may be given a meaning which is "repugnant" to the usual meaning of the term (see MPEP 2173.05). Here, "multi" cannot be given a meaning of "one" since this is repugnant to the usual meaning of "multi" as more than one (or two or more), and thus a "multiprocessor system" must include at least two processors in the system.]

On page 5, line 3, it appears "example" should be --exemplary-- for clarity. See also page 6, line 27.

On page 7, line 5, it appears --processors in-- should be inserted before "a set" for clarity and consistency (see Fig. 4, as well as page 8, line 29, for example). In line 24, the language "predicts a function" is confusing as it does not appear a "function" is predicted here. It appears

"function of the sets" should be changed to --set of predicted readers-- for clarity and consistency (see page 9, lines 8-12, e.g.). Also, it appears --function or-- should be inserted after "union" in line 25 for clarity and consistency (note page 8, line 7, e.g.).

On page 8, line 8, it appears --the-- should be inserted before "desired" for clarity. In line 29, it appears --of nodes-- should be inserted after "set" for clarity and consistency.

On page 12, line 24, it is not entirely clear what is meant by "expensive" in this context ("expensive" in terms of what? Money (cost)? Time?).

Again note that these are merely exemplary. The entire specification should be carefully and completely reviewed to ensure that all possible errors are located and corrected.

In the claims:

In claim 20, line 1, "wherein the" (either occurrence) should be deleted for clarity.

Appropriate correction is required.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-4, 10, 21-25, 28-31 and 34 are rejected under 35 U.S.C. 102() as being anticipated by Kaxiras ("Identification and Optimization ... Shared-Memory Multiprocessors").

With respect to claim 1, as well as claims 22 and 28, Kaxiras discloses a method and apparatus for determining a set of predicted readers of a data block in a multiprocessor system, the method including determining a current set of readers of a data block which is subject to a write request [Kaxiras teaches determining and collecting the identities of current "consumers" in a temporary bitmap (see pages 206-207, e.g.). Kaxiras discusses an SCI protocol as well as other directory based cache coherent protocols in which the directory itself keeps track of consumers using a full bitmap]. Kaxiras also teaches generating a set of predicted readers or consumers based on the current set of readers in the temporary bitmap and at least one additional set of readers representative of at least a portion of a global history of a directory associated with the data block [Kaxiras teaches that a set of predicted consumers or readers may be generated from the logical AND or intersection of the temporary bit map and a predictor bit-map. This "intersection prediction" predicts the intersection of the last two sets of consumers to be the new set of consumers or readers.) Again note that Kaxiras discusses an SCI protocol as well as other

directory based cache coherent protocols in which the directory itself keeps track of consumers using a full bitmap].

With respect to claims 2-3, as well as claims 23-24 and 29-30, Kaxiras teaches applying a "function" such as an intersection or logical AND function to the current set of readers and at least one additional set of readers (again see pages 206-207).

With respect to claim 4, as well as claims 25 and 31, Kaxiras teaches that the directory and the data block comprise elements of a memory associated with a processor node of the multiprocessor system.

With respect to claim 10, Kaxiras also teaches sending the resulting data block to each of the readers in the set of predicted readers [Kaxiras teaches speculatively "pre-sending" the data block to each of the predicted "readers" or consumers (see pages 208-209, e.g.).]

With respect to claim 21, as well as claim 34, Kaxiras teaches that a "subset" of the readers such as one reader corresponds to a particular processor node in the multiprocessor system (a bit in a bit map may be used for each of the processors).

6. Claims 5-7, 11-20, 26-27 and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaxiras.

With respect to claim 5, as well as claims 26 and 32, Kaxiras discloses a method of determining a set of predicted readers of a data block in a multiprocessor system including generating a set of predicted readers or consumers based on at least two sets of consumers

including a current set of consumers or readers and a previous set of consumers or readers, but does not teach that the history information comprise a plurality of sets of previous readers processed by the directory. However, one of ordinary skill in the art would readily recognize that maintaining more than one set of previous readers in the history information allows one to better track the history of the previous readers or consumers and improve the prediction ability of the prediction scheme. Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to store of a plurality of sets of previous readers in the history information of Kaxiras in order to improve the prediction ability and thereby improve system performance by more accurately predicting where to "pre-send" information.

With respect to claim 6, as well as claims 27 and 33, Kaxiras teaches that the prediction is made using sets of consumers such as the last two sets of consumers. As the sets of consumers change, the dynamic prediction scheme will apply a "function" to the previous two sets of consumers and different sets of consumers will replace the sets as new consumers sets are formed, i.e. the set of predicted consumers is not cumulative but it changes dynamically. Since the last two sets are used, the set previous in time to the last two sets will no longer be used and will be replaced or "shifted" out as time progresses. Thus, the global history may be considered to be maintained in a shift register having a number of storage locations corresponding to a designated history depth.

With respect to claim 7, as discussed above with respect to claim 5, the history depth may obviously be changed depending on the number of previous sets of consumers maintained and the desired degree of accuracy of the prediction scheme and the selection of a particular number of sets of previous consumers such as three or more sets would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made and, as such, does not render the claimed invention patentably distinct.

With respect to claim 13, as well as claims 14-17, Kaxiras discloses a method of determining a set of predicted readers of a data block in a multiprocessor system including generating a set of predicted readers or consumers based on at least two sets of consumers including a current set of consumers or readers and a previous set of consumers or readers, but does not teach that the function may be selected dynamically. While Kaxiras specifically only discusses an "intersection" or logical function, those of ordinary skill in the art would recognize that other logical operations or functions such as a logical OR (union) function may also be used depending on the bandwidth available and capacities of the memories. Kaxiras teaches that the prediction scheme should be dynamic so as to maintain optimum performance and the selection of a particular logic function dynamically such as on a per program or per page basis in order to optimize performance based on available bandwidth and other system considerations would have been readily obvious to one of ordinary skill in the art a the time the claimed invention was made.

With respect to claims 11 and 12, the selection of a particular update mechanism in order to optimize system performance would have been further readily obvious to one of ordinary skill in the art.

With respect to claims 18-20, Kaxiras teaches utilizing a hybrid prediction scheme and that protocols in which the directory is an excellent source of information about the consumers and the selection of particular types of information such as a subset of cache address information, processor node information and program counter information in order to optimize the hybrid prediction scheme would have been further readily obvious to one of ordinary skill in the art at the time the claimed invention was made and does not patentably define the claimed invention over the prior art.

7. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaxiras in view of Islam et al.

With respect to claims 8 and 9, Kaxiras discloses a method of determining a set of predicted readers of a data block in a multiprocessor system including generating a set of predicted readers or consumers based on at least two sets of consumers including a current set of consumers or readers and a previous set of consumers or readers, but does not teach maintaining an "accessed bit" for each of a plurality of data blocks, the accessed bit of a particular reader for a given data block indicating whether the particular reader has actually read the given data block.

Islam et al also discloses a shared memory multiprocessor system and teaches maintaining an "accessed bit" for each of a plurality of data blocks, the accessed bit of a particular reader for a given data block indicating whether the particular reader has actually read the given data block (see column 3, lines 44-47 and Figure 1b, e.g.). In this manner, feedback is provided as to whether the data block is actually being accessed so that the performance of the system such as a cache placement/replacement scheme may be tuned or optimized (by monitoring whether a data block put in a cache is actually accessed, better placement/replacement decisions may be made).

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to maintain an "accessed bit" for each of a plurality of data blocks, as taught by Islam et al, in the shared-memory multiprocessor system of Kaxiras, in order to obtain feedback on the actual use of the data and thereby improve system performance.

With respect to claim 9, it would have been obvious to send the accessed bit information with other status information such as validity/invalidity information so as to reduce the amount coherence traffic.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Koufaty et al ("Data Forwarding in Scalable ...") and Koufaty et al ("Comparing Data Forwarding ...") are cited of interest as disclosing data prefetching and data forwarding in shared-memory multiprocessor systems similar to the present invention.

Abdel-Shafi is cited as discussing producer initiated communications in a shared-memory multiprocessor system.

Kaxiras et al ("A Study of Three ...") is cited of interest as discussing coherence protocols and sharing data in a shared memory multiprocessor system.

Liu is cited as disclosing data prefetching in a multiprocessor system including a plurality of caches.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

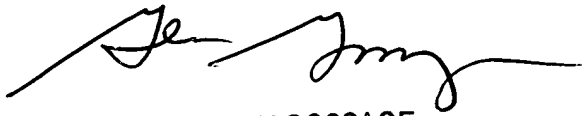
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (703) 308-1756.

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)
(703) 746-7239 (Official Communications)

(703) 746-5713 (Use this FAX number only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal paper/amendment be faxed directly to him or her on occasion.)



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